South Bay Circuits

Manufacturability Guidelines

FOR

Printed Circuit Boards

South Bay Circuits, Inc.
99 N. McKemy Ave
Chandler, AZ 85226

GL-1007

By: Edward (Eddie) Rocha

South Bay Circuits

Dear Customer,

The intention of this document is to provide information regarding the manufacturability of printed circuit boards. Understanding this information can help the designer control the cost by avoiding requirements that impact the cost whenever possible.

This information, by no means should be interpreted as a capabilities matrix. PCB designs falling outside the parameters described in this document can probably still be produced with special handling and attention. Although producible, these sorts of designs will cost more to manufacture.

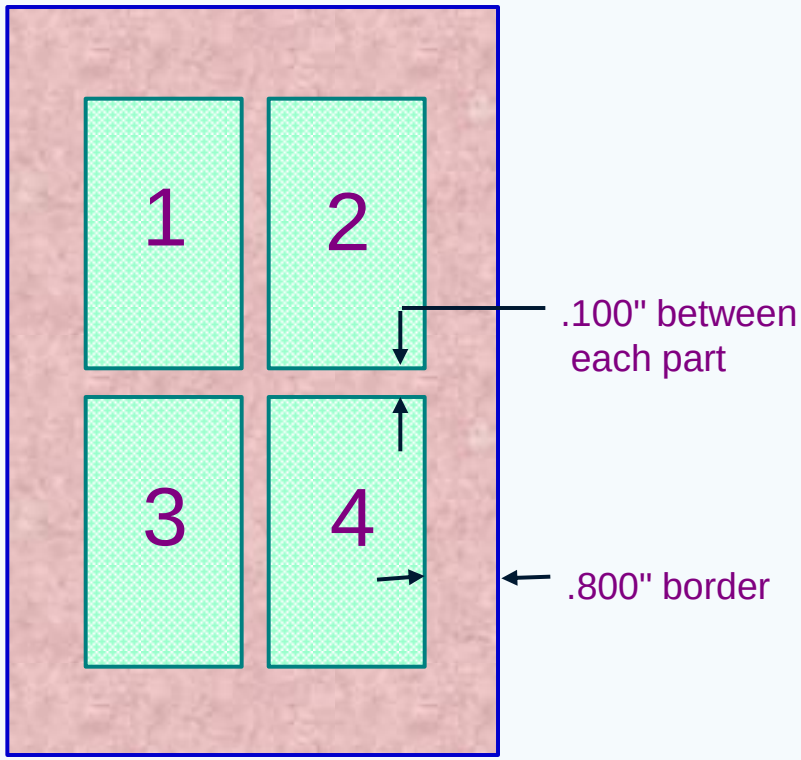
I hope this document provides information of value which can be utilized to all of our best interests, PCB assembler, PCB fabricator and end customer.

Thank you,

Edward Rocha
Director of Engineering
South Bay Circuits, Inc.
(480) 940-3125

Panelization

Process Panel



Boards are processed in multiples, on one process panel.

Since material is a major cost factor proper panel utilization is critical.

This illustration shows 4 individual PCBs on one process panel.

Boards are de-panelized using an N.C. route machine. Allowing .125 in. between parts allows the panels to be stacked at an optimum 4 high for each spindle.

* Double-sided (2 layer PCBs) require only a .500" border

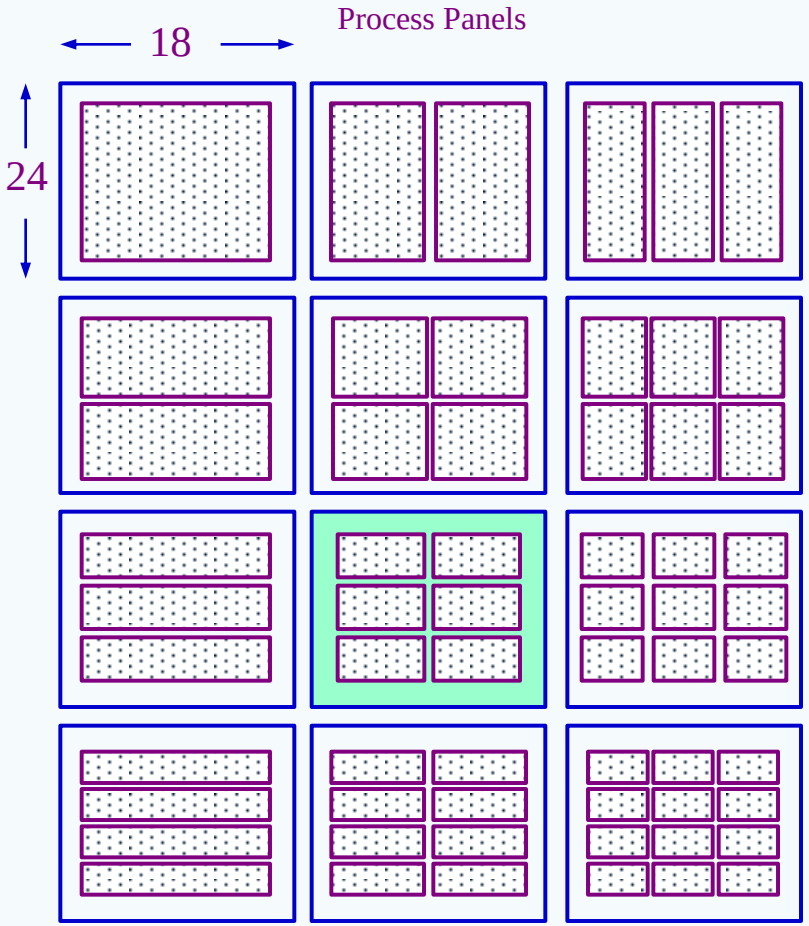
Panel Sizes

Panel Size	Usable Area
18 x 24	16.4 x 22.4 most cost effective
24 x 30	22.0 x 27.7 non-standard size

- 18 x 24 panels are the most cost effective panels for production orders

Panelization Matrix

Process Panel Dimension	Maximum Board Dimension	# of boards in axis
18.00	16.4	1
	8.15	2
	5.40	3
	4.02	4
	3.20	5
	2.65	6
	2.25	7
	1.96	8
24.00	22.4	1
	11.15	2
	7.40	3
	5.52	4
	4.40	5
	3.65	6
	3.11	7
	2.71	8
	2.40	9

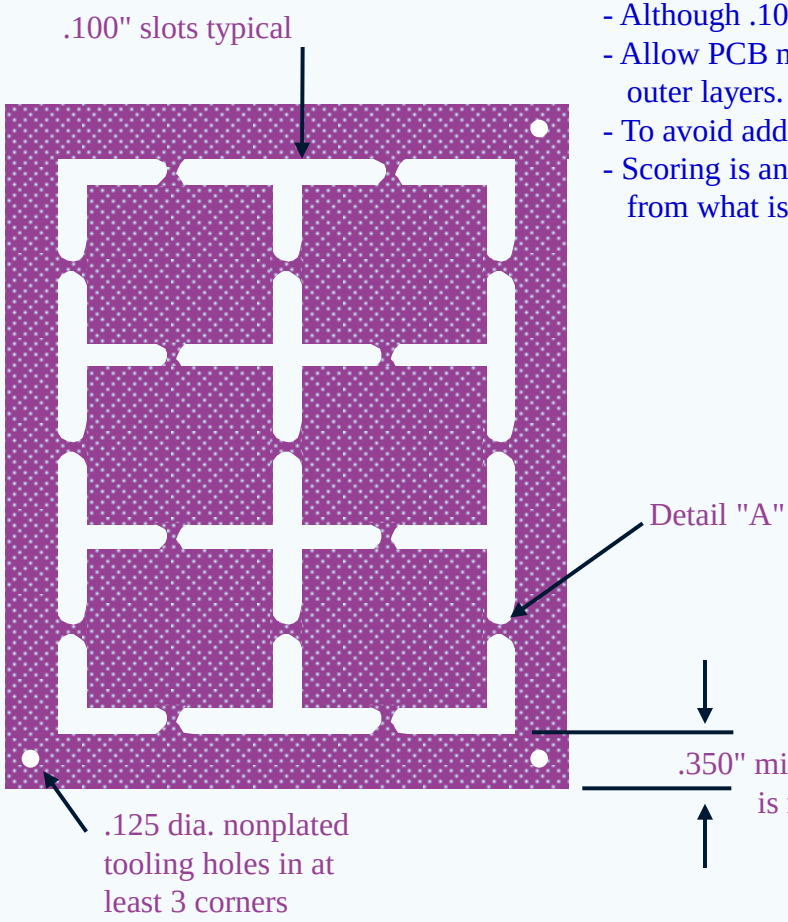


example: 6" x 8" PCB = 6 parts per process panel
6" fits 3 times in the 24" axis
8" fits 2 times in the 18" axis

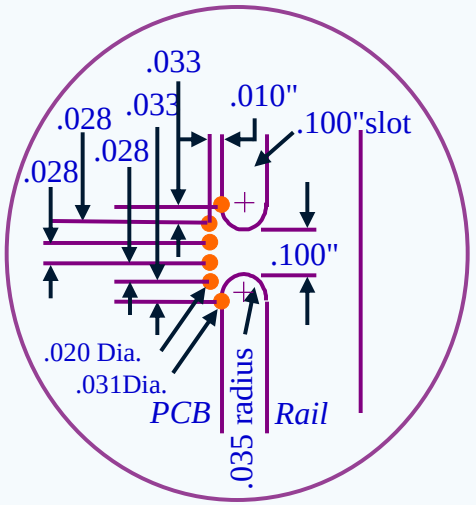
These parameters are for multilayers, 2-layer PCB's require only .500" border.
Boards smaller than 4 x 4 should be built and delivered in a breakaway array

Panelized Arrays

- Smaller boards may be shipped in an array form.
- Array panels allow for a more efficient assembly process.
- Shown below are some typical parameters for an array panel.
- Although .100" wide slots are common place, the preferred slot width is .125"
- Allow PCB mfg'r to add thieving patterns to the break-away rails inner layers as well as outer layers.
- To avoid additional costs avoid scoring when possible.
- Scoring is an additional process which involves additional set-ups on a machine different from what is used to route PCBs



Detail "A"

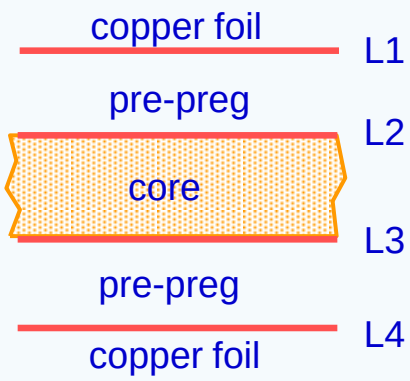


This approach leaves a mouse bite, approx: .020" into PCB

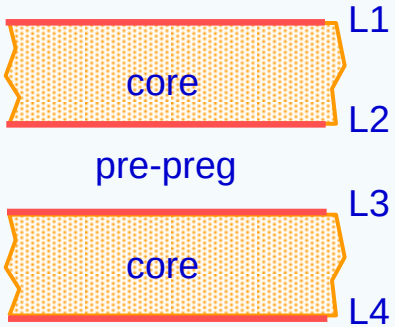
Multilayer Constructions

- Multilayer PWBs consist of three different components: copper foil, pre-preg, and core material. Pre-preg is the dielectric material between each conductive layer.
- Pre-preg is a woven glass coated with resin. The pre-preg is in a partially cured state (B-stage) to allow for handling and storage.
- Core materials are copper clad laminates constructed of a ply/plies of pre-preg with copper foil laminated on both sides, fully cured (C-stage).
- There are two types of constructions for multilayer PCBs: Core & Foil constructions. Foil constructions are more cost effective to build.
- Foil constructions also aid in yielding flatter PCBs

Foil Construction



Core Construction



Base Copper

- The amount of base copper is referred to in ounces per square foot. There is a direct correlation between the copper weight and the thickness.

Nominal Weight	Nominal Thickness	
1/8 oz	.00020	Non-standard
1/4 oz	.00036	
1/2 oz	.0007	
1 oz	.0014	
2 oz	.0028	

- External layers with half oz copper and internal layers with 1 oz copper are preferred.
- Internal signal layers with lines less than .005" wide should be processed on half oz copper.
- Internal plane layers on 1 oz copper are more cost effective than 2 oz plane layers.
- A minimum of 10 mil spacing between conductors should be maintained when using 2 oz copper

(A 2 oz copper requirement could add as much as 20% in material costs)

Dielectric Material

FR4 is our standard type of material. This material is certified to IPC - 4101.

Glass Transitional Temperature - - - - - -	170C
Dielectric Constant (1GHz) - - - - - - - - - - - - -	5.2
Flammability Rating - - - - - - - - - - - - - - - - - -	94VO

Laminates (class B/L)

.002 core +/-.0010	.012 core +/-.0015
.003 core +/-.0010	.014 core +/-.0020
.004 core +/-.0010	.018 core +/-.0020
.005 core +/-.0010	.022 core +/-.0025
.006 core +/-.0015	.028 core +/-.0025
.008 core +/-.0015	.038 core +/-.0040
.010 core +/-.0015	

Pre-pregs

106	.002	+/-.0005
1080	.0027	+/-.0005
2113	.004	+/-.0005
2116	.005	+/-.0005
7628	.007	+/-.0010

South Bay Circuits will maintain a +/-.0025" dielectric tolerance when using a pre-preg combination.

* *Many in the industry are beginning to require higher temperature materials (around 170 Tg) when the design has a high aspect ratio and/or a high quantity of layers. This is to reduce the z-axis expansion in the PTHs making a more reliable PTH.*

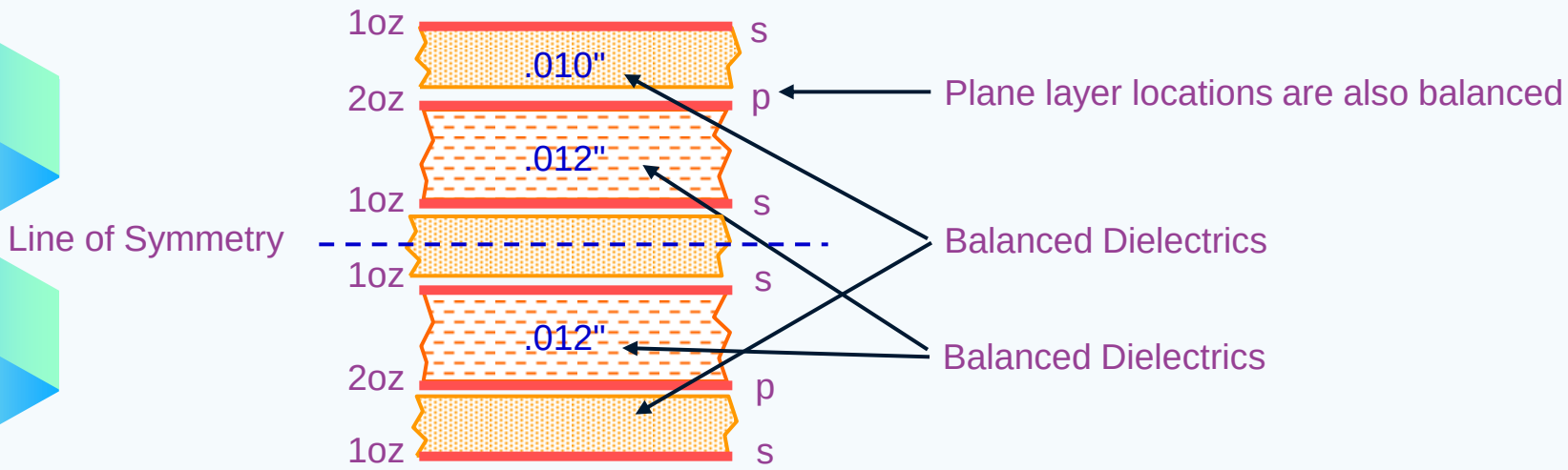
Lead Free Materials

- Standard FR4's are RoHS compliant but not necessarily compatible with all lead-free assembly processes
- Four material characteristics desired for lead free assembly are shown below. Also shown are laminate products that are RoHS complaint and compatible with lead-free processes

	Tg	Td	Z-axis expansion	CAF IPC-TM-650 2.6.25
Isola 370HR	180	340	2.8	Yes
Grace GA-170-LL	175	350	2.5	Yes
Panasonic R-1755S	175	364	2.7	Yes
Ventec VT-47	175	345	2.8	Yes

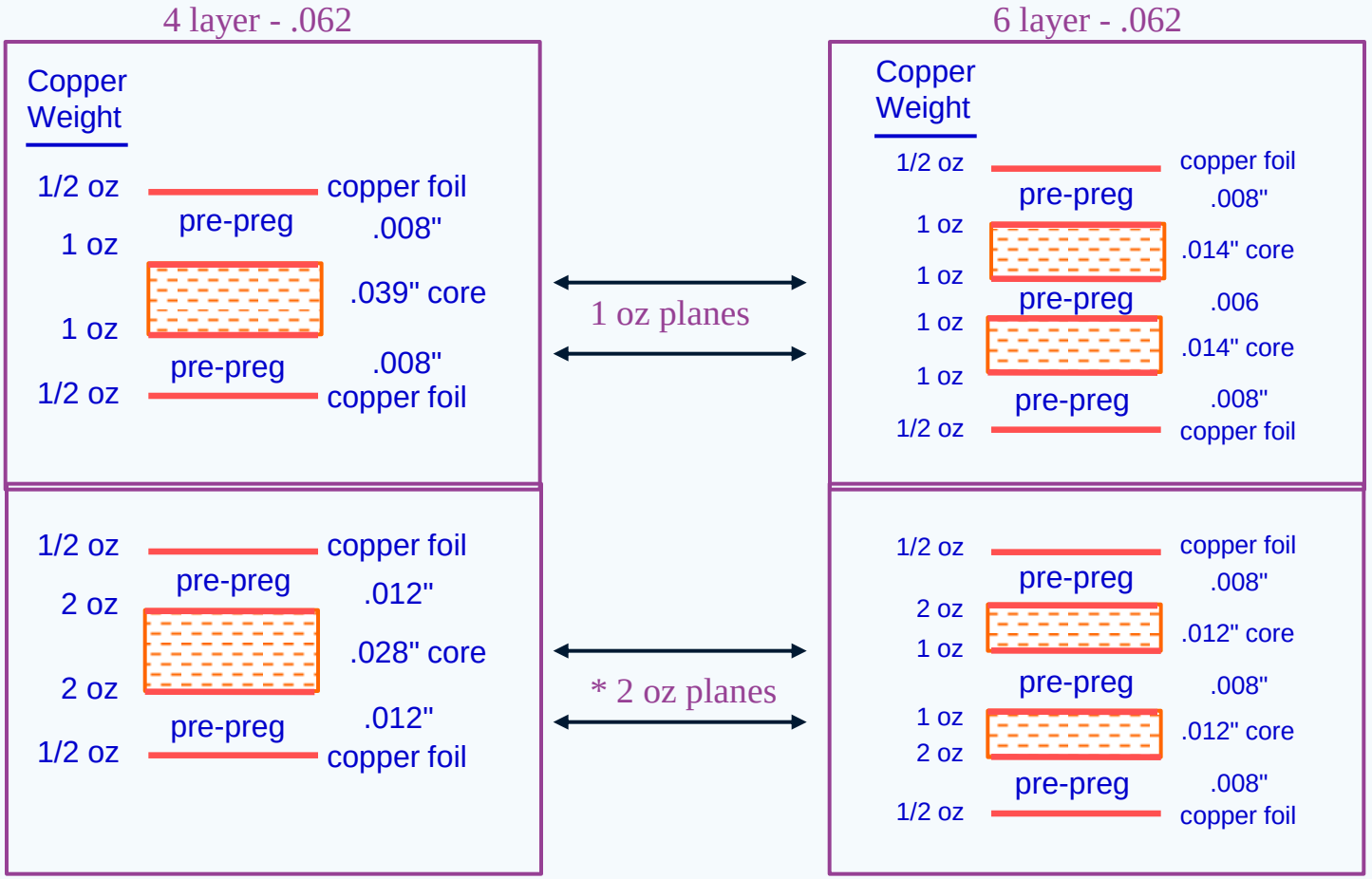
Balanced Constructions

A balanced construction is vital for achieving a flat printed circuit board. Shown below is a construction where the copper weights of the material and the dielectric spacings are balanced. In addition, the copper layout within a layer being balanced, helps yield a flat PCB. A balanced board construction as shown in the example below will help in avoiding warpage problems.



Standard Constructions

Multilayer PCB constructions should be symmetrical. A non-symmetrical construction could create warpage issues. Shown below are some typical constructions.

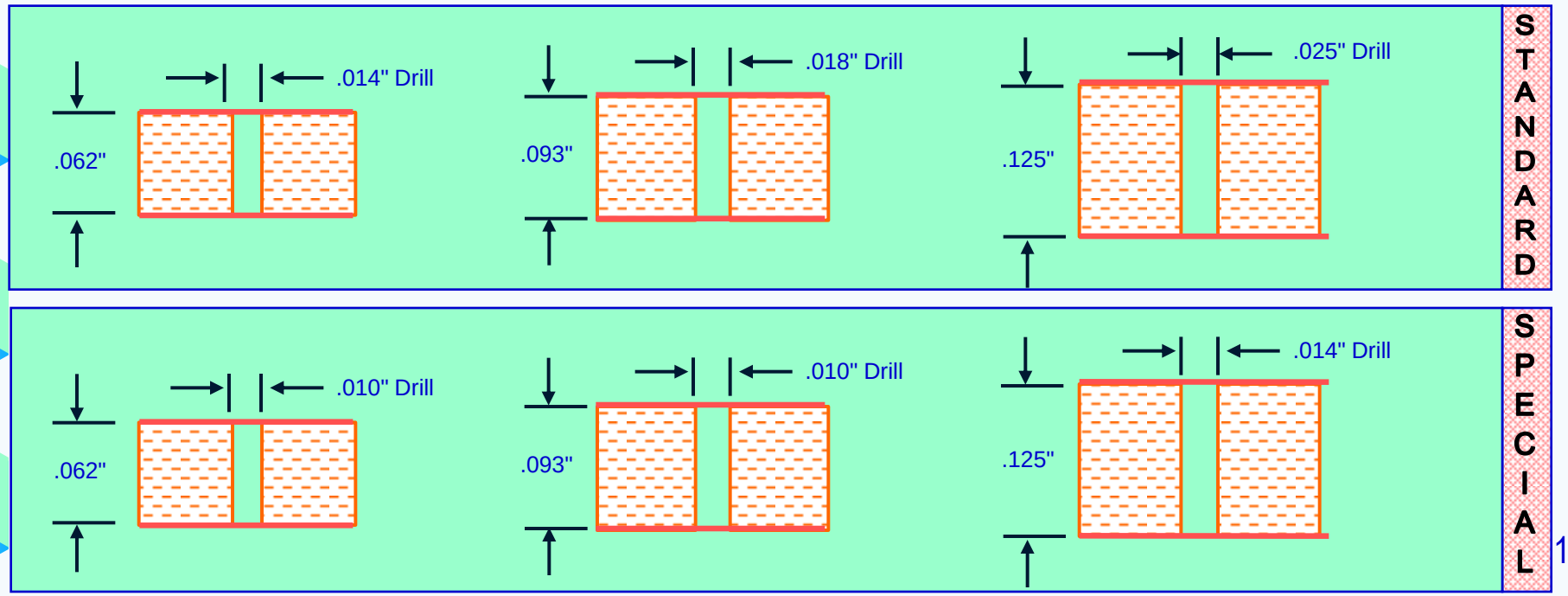


** 2 oz plane layers add approximately 20% to the material cost of the board .*

Aspect Ratio

Aspect ratio describes the relationship between the PCB thickness and the smallest drilled hole. This ratio is critical in allowing proper plating of the hole. Aspect ratios of 5:1 are typical, higher aspect ratios can impact the cost of the board. As the aspect ratio goes up so should the consideration to use a high temperature FR4 material (170 Tg). With high temperature FR4 material there's less z-axis expansion when exposed to thermal processes. Z-axis expansion introduces stress on a plated barrel of the hole and presents a risk of barrel cracking (symptom would be an intermittent open in the via).

Aspect Ratio = Board Thickness / Drilled hole



Pad Sizing

This is an area where discrepancies are common. The formula below can be used to determine pad sizes for plated-thru component holes.

PAD SIZE = FHS + .017"

FHS: nominal finished hole size

Today via pad sizes must be smaller than what this formula determines. Smaller pads are needed to meet current density requirements. The smallest cost effective via is drilled with a .014 drill diameter and it should have a .025 pad, which can still achieve a .002 annular ring at the junction if teardropping is permitted

To ensure sufficient isolation from internal plane layers, anti-pads can be determined with the following formula.

Inner layer anti-pad size = FHS + .025”
Outer layer anti-pad size = pad size + .016”

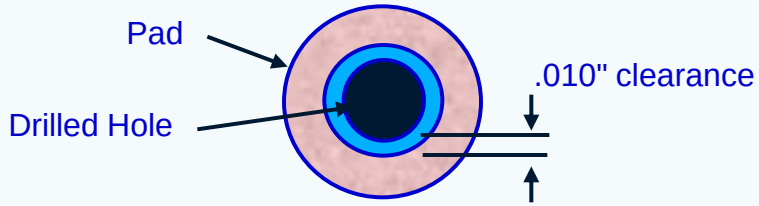
Inner layer anti-pads should be no smaller than .030

THERMAL RELIEFS

INSIDE DIA. = PAD SIZE
OUTSIDE DIA. = I.D. + .020"
TIES (minimum) = .010"

Removal of non-functional pads on internal layers is recommended.

Having no pads for non-plated holes is preferred. This allows the PCB fabricator to “TENT” the hole and avoid a secondary drill operation. If a pad is required, a .010" clearance of the hole will still allow for tenting.

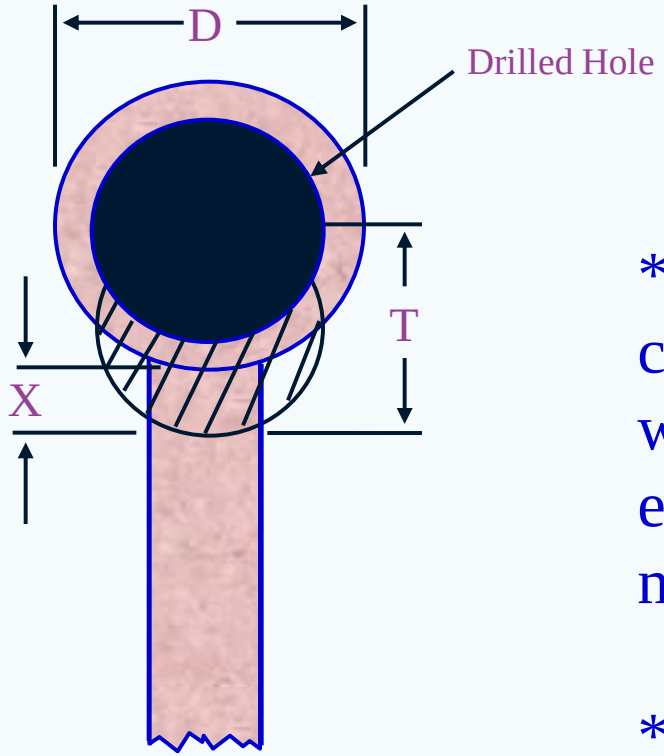


The New Smaller Vias

- Increasing densities require smaller vias
- Hole sizes are being specified down to 8 mils
  - Excluding micro-vias (HDI Technology)
  - PCB fabricators will drill with the most cost effective drill diameter
    - Annular ring is targeted not the finished diameter
- The finished hole size is not critical (+.003/ - dia)
  - Insertion not required
  - Interconnect is the goal
- Choice of drill diameter is key
  - Maintain annular ring
  - Must be able to plate
  - Drill diameters less than .0135 add cost

Pad size	Drill dia.
.025	.0135
.020	.012
.018	.010

Teardrops



D = Pad Diameter
T = Teardrop Diameter
X = Extension

* The teardrop provides a reliable connection of the plated thru-hole with any conductor routed to that hole, even in cases where the hole is mis-aligned.

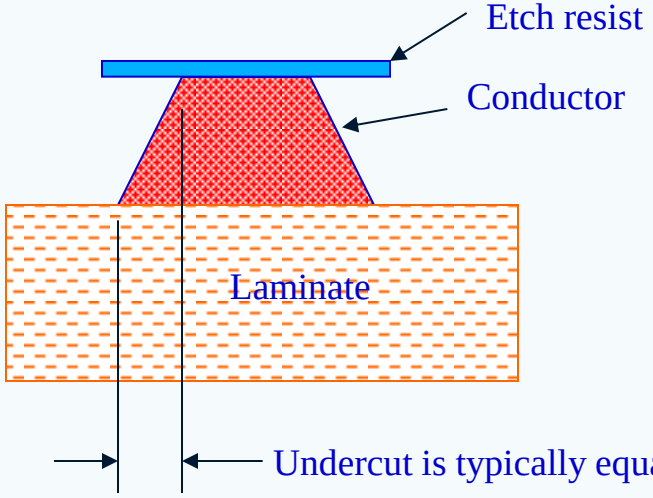
* Most all CAM softwares have teardropping features which will maintain minimum spacings required by the customer.

Trace Widths

	Acceptable	
Minimum Trace Width	.004"	artwork values
Associated Spacing	.004"	no etch compensation
Tolerance	+/-.001	

**Half oz. copper is req'd, both for external and internal layers*

- Although etching fine lines on external layers is more challenging to produce than those on internal layers the capability is pretty much the same
- Half oz. base copper is preferred on outer layers
- A thicker copper limits fine line capability
- Producing lines less than 3 mils requires a different manufacturing approach altogether
- Signal layers using 2 oz copper should be limited to designs with non-critical lines of 15 mils or greater



To compensate for etching undercut, artwork trace widths are increased. Artwork for designs which begin at 4 mil spacing are not compensated. Etching circuitry with spacing less than 4 mils becomes a non-standard design and will add cost.

Copper Thickness	A/W Compensation
.5 oz	.5 mils
1 oz	1 mil
2 oz	2-3 mils

Trace Routing

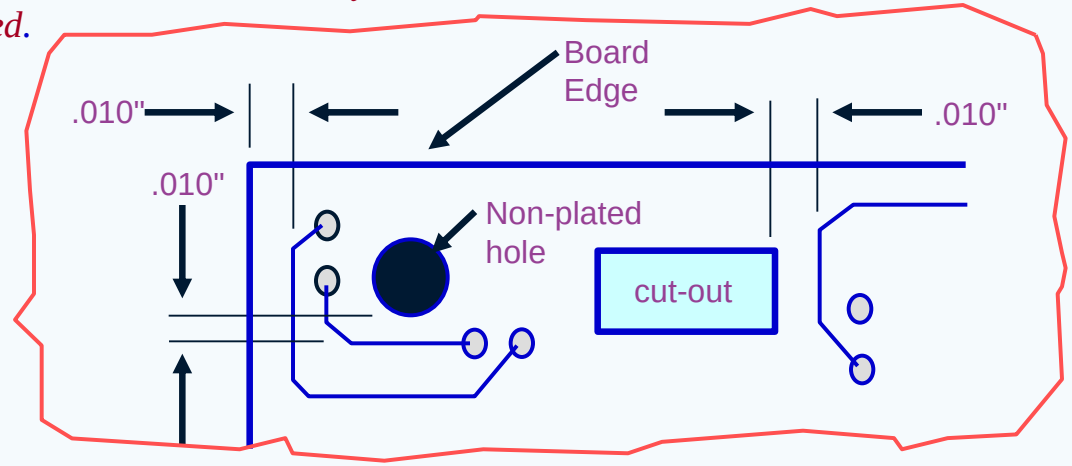
- It is important to balance the circuit pattern across the board
- On the external layers it helps achieve a uniform plating
- On the internal layers it helps avoid potential warpage issues
- Areas with isolated circuits should be surrounded by thieving patterns
  - This will balance the pattern to be plated and achieve a more consistent plating.

The thieving patterns are either square .080" non-functional pads on .100" centers, or round .080" non-functional pads on .100" centers.

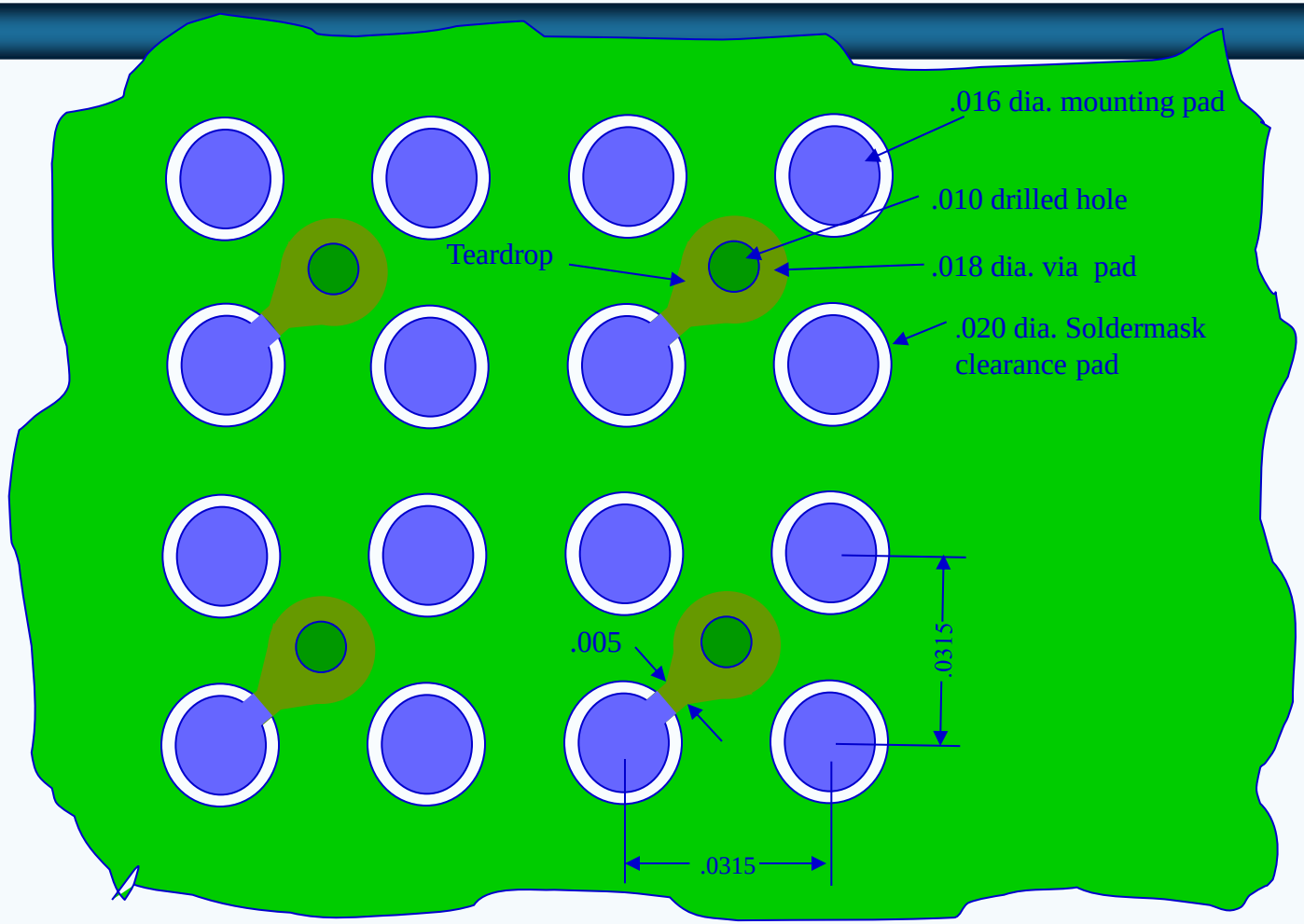
Spacings

- Trace to board edge spacing should be no less than .010" (cut-outs included).
- Trace to hole spacing should be .010", the edged of any drilled hole to the edge of any conductor. This would include both plated and non-plated holes.
- Drilled hole edge to drilled hole edge spacing is to be no closer than .012

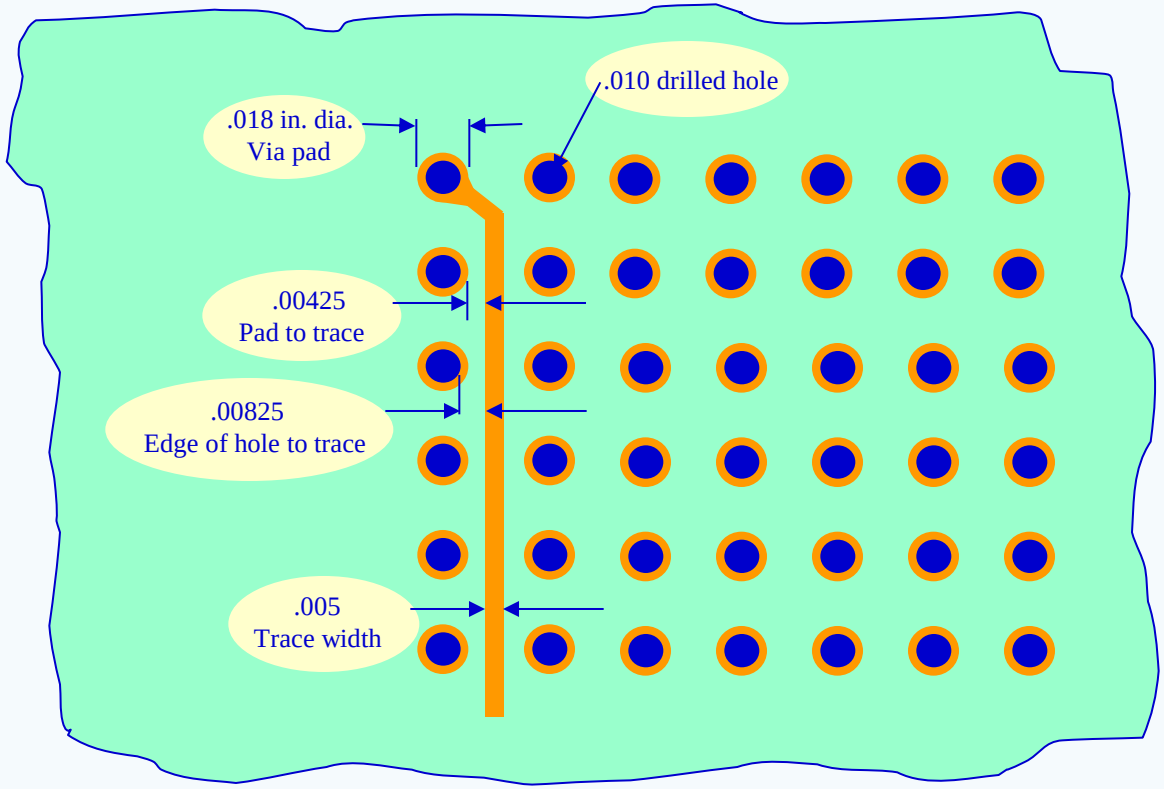
** Many of todays designs are beginning to violate this rule(i.e. .8 mm BGA's) The densities are driving the minimum spacing down to .008". Not all PCB fabricators are able to deal with this .008" hole-conductor spacing so only use it when required.*



.8 mm BGA External layer

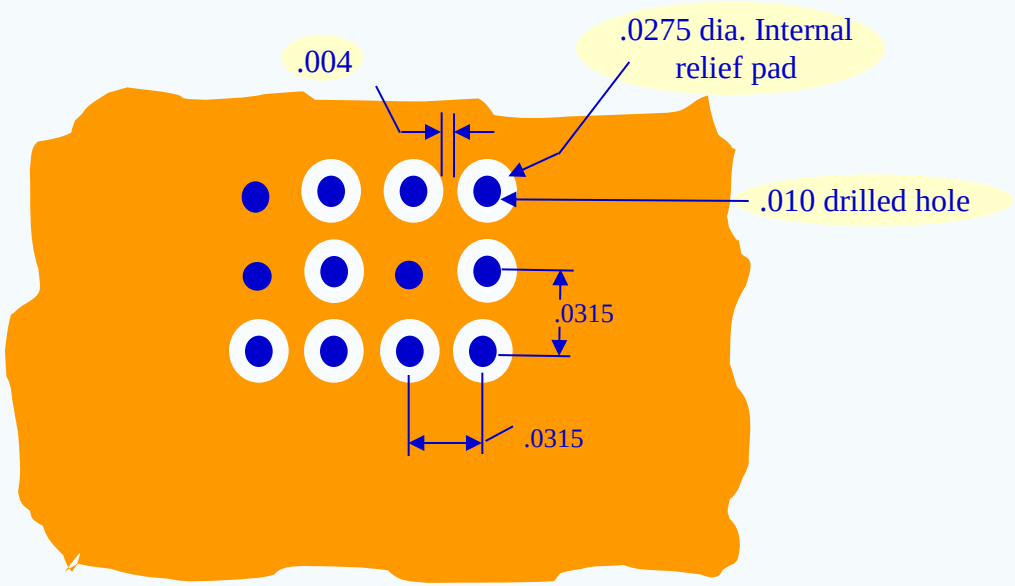


.8 mm BGA Internal Signal layer



These values are gerber values and not values of the finished product. The finished product will yield .004 in. traces

.8 mm BGA Internal Plane



Via Fill

-Via filling is typically used when via-in-pad is utilized and the via is a thru-hole **OR** for heat dissipation purposes.

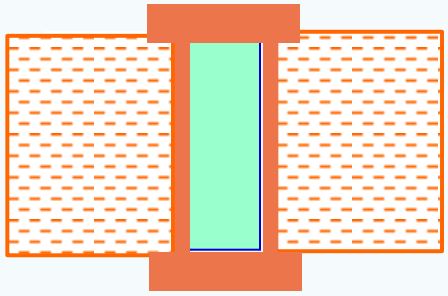
Via filling involves several additional fab processes

- Multiple plating processes
- Selective plating
- Multiple drilling processes

Via filled thru-hole

Options are conductive or non-conductive

(non-conductive filling is preferred due to better CTE characteristics)



Controlled Impedance

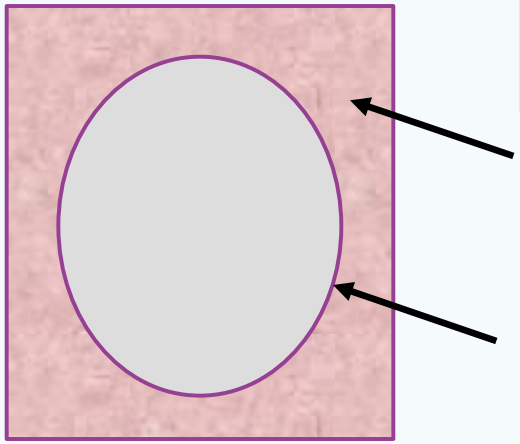
- Controlled impedance is very common
- Critical factors are:
  - Conductor width
  - Conductor height
  - Dielectric spacing
  - Dielectric Constant
- Controlling the conductor width is aided by using the proper copper weight
  - .5 or 1 oz for internal layers
  - .5 oz for external layers
  - 2 oz is strongly discouraged, etch control for thick copper is not as consistent
- Tolerance of +/-10 % is typical (+/- 5 ohms is the tightest tolerance)

DOCUMENTATION

- Dielectric spacing should be referenced on the drawing with no tolerance
  - Indicate "Reference Only"
  - Flexibility for the PCB fabricator to meet the requirement
- Specify which conductors are to be impedance controlled
  - Do this on the drawing by indicating the conductor by its width
  - Indicate on which layer the conductor is
    i.e. " 5 mil lines on layers 1 and 6 are to be 50 ohms +/- 10%"
  - If differential impedance is required also indicate the conductor spacing between the impedance pair (or the pitch)
  - In the gerber files, the aperature for impedance lines should be separate from non-impedance lines.

Copper Plating

- An electrolytic plating method is used to deposit copper onto plated features and into plated-thru holes
- Variables which affect the copper thickness are:
  - plating time
  - amperage
  - feature to be plated
  - location of the plated feature within the panel



Plating Distribution
(within a process panel)

High Current Density Area
This area of the panel plates faster than the low current density areas

Low Current Density Area

- The industry standard for copper plating in the hole is .001" minimum average
- Measurements less than .001" (but greater than .0008") are acceptable
- This copper plating thickness will provide a reliable plated-thru hole
- Plating copper thicknesses greater than .001" may introduce processing issues for the PCB fabricator
- Problems arise in the plating , resist strip, etching, and soldermask operations

Surface Finishes

* OSP and White Tin are not offered by SBC

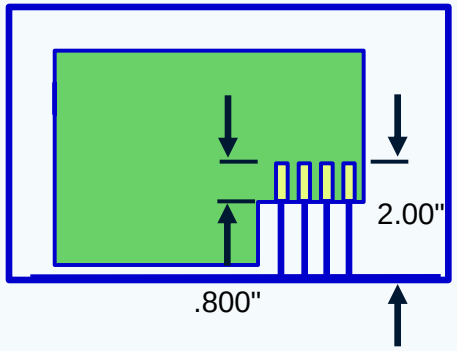
- **Hot-air-solder-level (HASL)** process involves:
  - Immersing the PCB panel in a bath of molten solder
  - Temperatures equal to that of a wave solder
  - 2-4 second dwell time
  - Air knives blow off the excess solder as the panel exits

  The solder thickness achieved can range from .000050" - .0015".
- **Electroless Nickel / Immersion Gold (ENIG)** provides a flat surface finish which with today's fine pitch SMT and BGA devices will be required. This is a solderable surface with an excellent shelf life.
- **Silver** is another surface finish which provides a flat solderable surface. This surface finish is sensitive to handling more so than ENIG. White polyester gloves are recommended when handling silver PCB's. PCB's must be properly stored in a way that they are not exposed to a high humidity environment (>65%). Avoid contacting paper containing sulfur.
- **Organic Solderability Preservative (OSP)** is a surface finish which basically leaves a copper finish which is protected from oxidation. The surface is flat and solderable. It too is sensitive to handling and requires white gloves.
- **White tin** is yet another finish that provides a flat solderable surface. And it too should be handled with white (polyester) gloves. No baking of PCB's with white tin is allowed, this is detrimental to solderability. This finish has not been too popular due to the extreme sensitivity to handling.

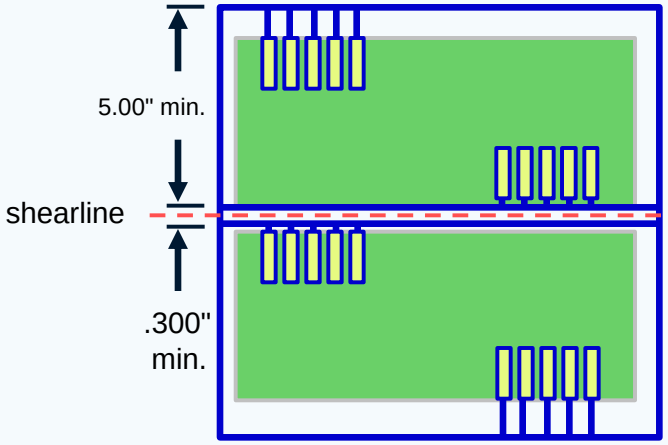
No longer are the solder thickness variations and coplanarity issues associated with HASL acceptable for assembly of today's fine pitch and high density packages. Assemblers need a flat and solderable finish which can survive multiple thermal excursions. All finishes except HASL meet these requirements and are compatible with the lead free assembly process.

Gold Plated Edge Connectors

- Gold plating can be performed in an electrolytic bath where an entire photo-defined image is gold plated with a nickel layer beneath
- This approach is costly to maintain
- Edge connectors are typically plated on “Gold Tipping Lines” which are cost effective for this application
- The maximum distance between the top of any connector finger and the board edge should be 2.00". The maximum length of a connector finger should be .800".



- Boards with gold connector fingers along two different edges of the board, will require shearing of the process panel prior to gold plating.
- Minimum panel width to run down a conveyorized gold tab plating line is 5.00".



- **.000100" of nickel** and .000030" of gold is typical.

Soldermask

-Soldermask is the external coating of the PCB, which typically defines the areas that will be soldered
-(ie: SMD pads, component holes, etc.).

- The most common type of soldermask is **Liquid Photoimageable (LPI).**

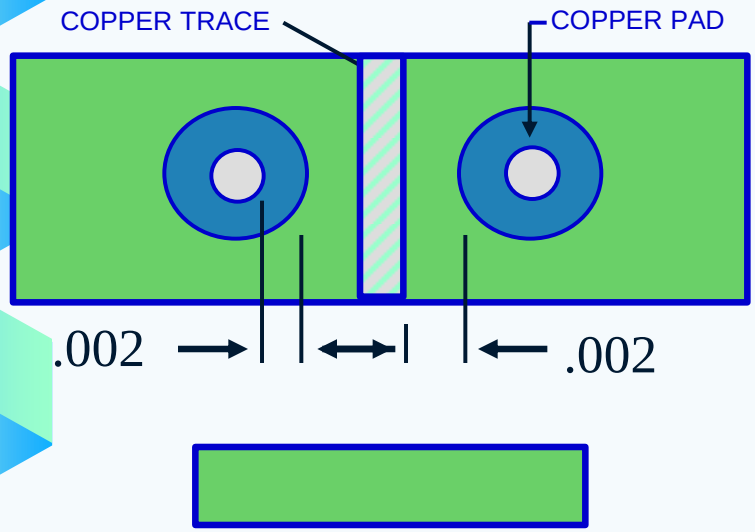
- Coating is a semi-automated operation
- Accuracy of a photo defining process
- Thermal cure

Available Colors: Green, Clear, Blue, Black, Red

Typical thickness: .0007” - .0012”

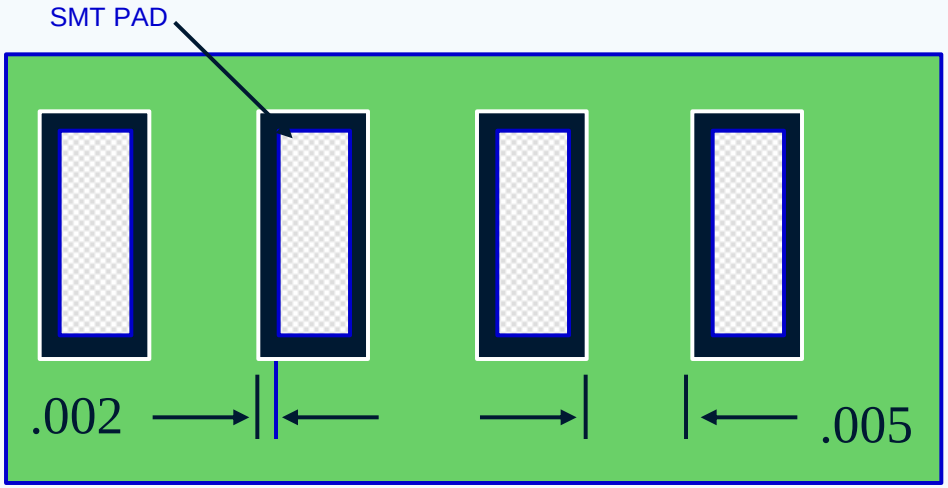
Soldermask Design - LPI

LPI soldermask Design Parameters



Soldermask Coverage

Surface Mount Technology



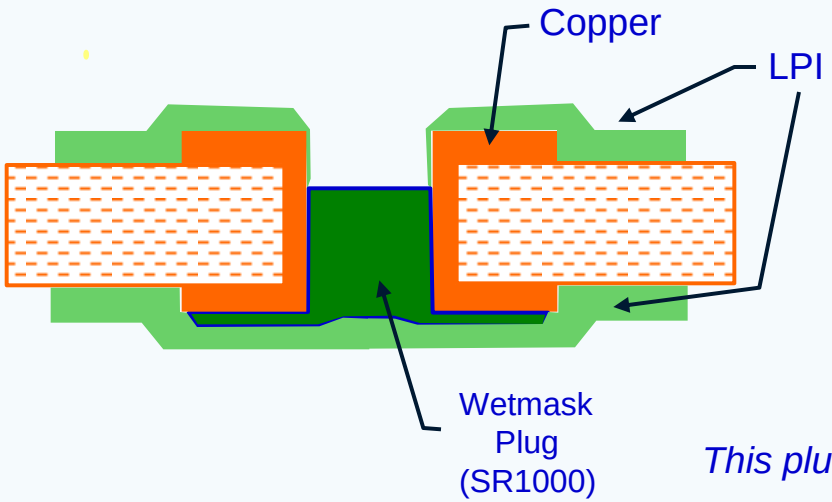
Dams help avoid solder bridging between SMT pads.

Wetmask Via Plugging

This should only be used if a vacuum draw is needed for in-circuit testing. If the vias are plugged in effort to prevent solder bridging, then mask up onto the via pad would be a sufficient alternative.
With via diameters less than .012”, a screened via plug process is not required because the LPI soldermask is capable of plugging the hole.

A plugging mask file can be generated by CAM. This file would include all the vias but not the test points. SR1000 is screened from the BGA mounting side or from the bottom side of the board if no BGA’s are present.

Screen Wetmask → LPI Process → HASL



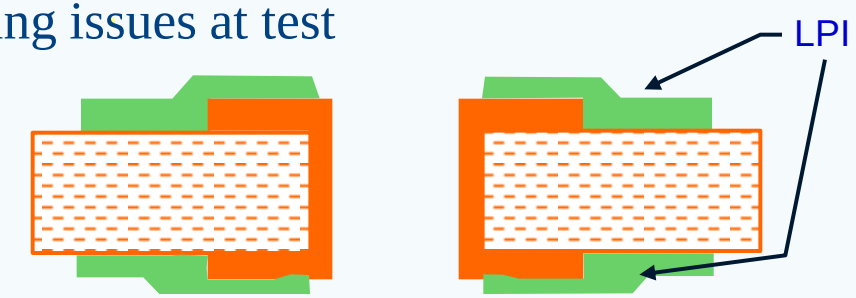
This plugging approach is for vias with an .020" dia. or less (drill)

Plated holes covered with LPI

-PTH's should either be covered with soldermask on both sides or open on both sides

- ENIG boards: barrel of hole (dia greater than .010) should be left clear of soldermask whenever design allows

- Open on one side of the board and covered on the other side, presents challenges to the fabricator
  - Surface discoloration
  - Non-uniform surface finish
  - ENIG plating issues
  - Probing issues at test

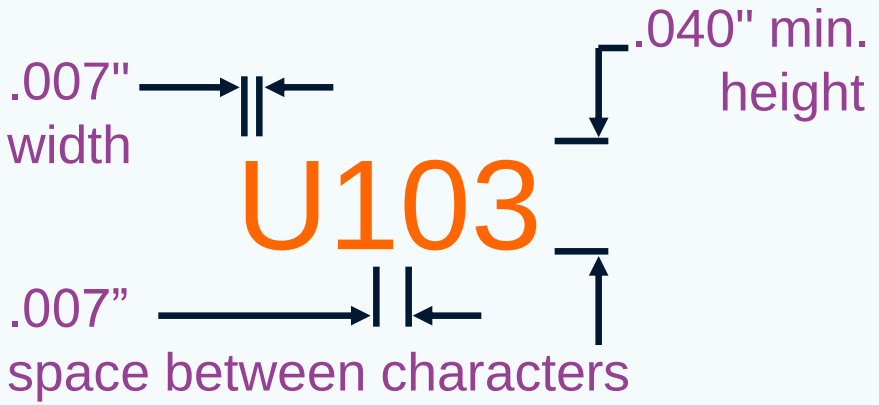


Best approach to cover vias for ENIG boards
Soldermask up on the pad but not in the hole

Silkscreened Legends

Legends are manually silkscreened using non-conductive epoxy ink. This process is not very accurate as far as registration or resolution. Legibility of characters is dependent on the character size. The minimum character height should be .040" with .007" spacing between characters. The optimum line width should be .007". If the spacing between characters is less than .007" than the height should be no less than .045". Legend should be clipped from all component pad surfaces. This should be considered when laying out the legend if legibility is to be maintained.

Optimum Character Dimensions



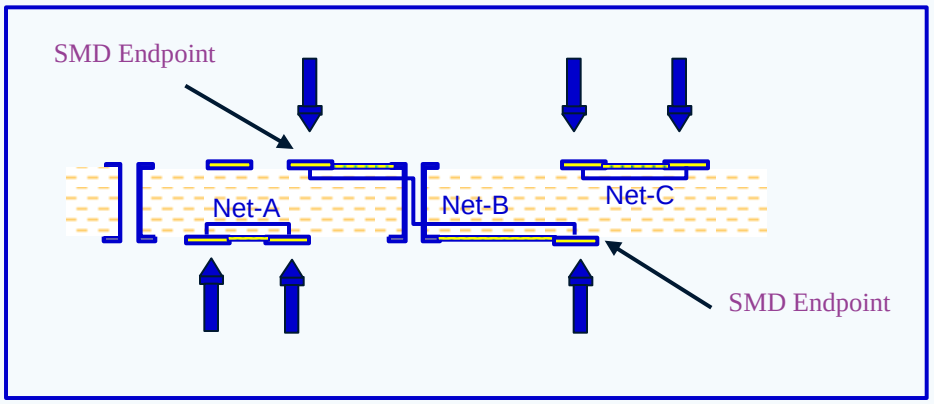
Electrical Test

- Electrical test should be performed on all PCBs to ensure no opened or shorted circuits are present.
- South Bay Circuits performs a bed-of-nails electrical test on all boards prior to shipping.
- Clamshell testing is now the norm for 2-sided SMT PCBs
- CAD Netlist Data is compared to the gerber netlist before the netlist is used on the test machines

Typical Test Parameters

Voltage	100V
Max. test pts.	42,000
Grid	.100"
Resistance (shorts)	10 M ohms
Resistance (opens)	20 ohms

Clamshell Test



(minimum pad dimension: .010 x .040")

De-panelization

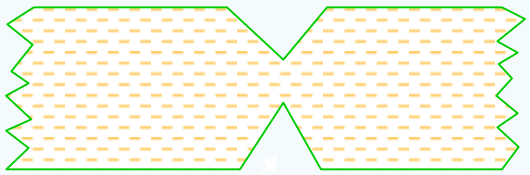
	Typical	Special
Minimum Inside Radius	.047"	.015"
Routing	+/-.005"	+/- .003"

An .047 radius is achieved by using an .093 router bit. This bit is most cost effective choice for the fabricator. Smaller bits can be used but the panel stack height must be reduced and the bit speed is slower.

Router bit diameter	Optimum Stack height	Tolerance Capability
.093	4 panels	+/- 005 4 Hi
.062	3 panels	+/- .003 2 Hi
.031	1 panel	+/- .003 1 Hi

Scoring

Remaining Thickness	+/-.005"
(maximum score depth: .025")	
Positional Accuracy	+/-.005"



30 Degrees

SMT devices should be no closer than .040" of the score line. Stress during the breaking away may introduce solder joint breaks. Scoring allows for zero spacing between boards when panelized on an array panel.